SUPPORT FOR THE AMENDMENTS

This Amendment cancels Claims 8-9; amends Claims 1-2, 4-6, 10-14; and adds new Claims 17-27. Support for the amendments is found in the specification and claims as originally filed. In particular, support for Claims 1, 4, 5, 13, 20 and 24 (e.g., "the first layer has a thickness dimension so that a depleted layer developed from the second layer when no electric voltage is applied to the gate electrode expands up to a surface of the first layer at a side where the gate electrode is located") is implicit in the specification at least at [0029] lines 4-10. Support for Claims 18, 19, 22, 23, 26 and 27 is found at least in Figs. 7, 8, 9 and 11. It is believed that no new matter would be introduced by entry of these amendments.

Upon entry of these amendments, Claims 1-2, 4-6, 10-15 and 17-27 will be pending in this application. Claims 1, 4, 5, 10, 12 and 13 are independent.

REQUEST FOR RECONSIDERATION

Applicants respectfully request entry of the foregoing and reexamination and reconsideration of the application, as amended, in light of the remarks that follow.

Applicants thank the Examiner for the courtesies extended to their representative during the personal interview on June 5, 2006.

As discussed at the personal interview, the present invention relates to a semiconductor device comprising a group III nitride semiconductor. In contrast to conventional semiconductor devices comprising a group III nitride semiconductor, the device of the present invention has an increased voltage resistance and a decreased ON resistance. Specification at [0005].

Claims 1 and 2 are rejected under 35 U.S.C. § 102(b) over JP 10-223901 ("JP-901"). JP-901 discloses in Figs. 9 and 11 a first layer (23b, 33b) comprising a group III nitride semiconductor, a second layer (23a, 33a) comprising a group III nitride semiconductor, and a

gate electrode (7). The first layer (23b, 33b) is provided between the gate electrode (7) and the second layer (23a, 33a). The channel is formed in at least one of: (i) the first layer (23b, 33b), (ii) the second layer (23a, 33a), (iii) the layer between the first layer (23b, 33b) and the second layer (23a, 33a) when electric voltage is applied to the gate electrode. The first layer (23b, 33b) is non-doped GaInN, and the second layer (23a, 33a) is n-type GaN. When the channel is formed, electrons flow through the channel.

However, JP-901 fails to suggest the independent Claim 1 limitations of a "semiconductor device comprising: a first layer comprising a group III nitride semiconductor, a second layer comprising a group III nitride semiconductor, and a gate electrode, wherein the first layer is provided between the gate electrode and the second layer; wherein a channel is formed in at least one of: (1) the first layer, (2) the second layer, (3) the region between the first layer and the second layer when electric voltage is applied to the gate electrode; wherein the conductivity type of the second layer is **inversed** with respect to the conductivity type of ***majority*** **carriers** that flow in the channel, and ...". When the conductivity type of the second layer is inversed with respect to the conductivity type of the majority carriers that flow in the channel, accumulation of carriers of the inversed conductivity type in the semiconductor device can be suppressed. Specification at [0007] and [0033].

Because JP-901 fails to suggest all the limitations of independent Claim 1, the rejection over JP-901 should be withdrawn.

Claims 1-2, 4-6 and 8-16 are rejected under 35 U.S.C. § 102(e) over U.S. Patent No. 6,933,544 ("Saito"). Saito discloses in Figs. 9 and 10 a semiconductor device comprising a first layer (2) comprising a group III nitride semiconductor, a second layer (9) comprising a group III nitride semiconductor, and a gate electrode (6), where the first layer (2) is provided between the gate electrode (6) and the second layer (9). A channel is formed in at least one of: (i) the first layer (2), (ii) the second layer (9), (iii) the region between the first layer (2)

and the second layer (9) when electric voltage is applied to the gate electrode (6). The first layer (2) is n-type AlGaN. The second layer (9) is p-type GaN. Between the first layer (2) and the second layer (9) is a channel layer (1) with a thickness set to about **1 to 2 μm**. See, Saito at column 3, line 34.

However, Saito fails to suggest the limitation of independent Claims 1 and 13 that "the first layer has a thickness dimension so that a **depleted layer** developed from the second layer when no electric voltage is applied to the gate electrode expands up to a surface of the first layer at a side where the gate electrode is located".

Saito also fails to suggest the limitation of independent Claims 4 and 5 that "the first layer and the third layer have the thickness dimension so that a **depleted layer** developed from the second layer when no electric voltage is applied to the gate electrode expands up to a surface of the first layer at a side where the gate electrode is located".

Saito also fails to suggest independent Claim 10. The field-effect transistor of Saito shown in Figs. 9 and 10 comprises a gate electrode (6), a first layer (2) comprising a group III nitride semiconductor of a first conductivity type, a second layer (9) comprising a group III nitride semiconductor of a second conductivity type located on a side of the first layer (2) opposite to the gate electrode (6), a third layer (1) located between the first layer (2) and the second layer (9) and electrodes (4-5) in contact with the first layer (2) and the second layer (9).

However, Saito fails to suggest the independent Claim 10 limitation that "the third layer has a band gap smaller than the band gaps of the first layer and the second layer". When the band gap of the third layer is smaller than the band gaps of the first layer and the second layer, the third layer becomes a recessed portion (quantum portion) so that the degree of electron collection increases. Specification at [0043]. As a result, the field-effect transistor of Claim 10 has decreased ON resistance.

Saito also fails to suggest independent Claim 12. The field-effect transistor of Saito shown in Figs. 9 and 10 comprises a gate electrode (6), a first layer (2) comprising a group III nitride semiconductor of a first conductivity type, a second layer (9) comprising a group III nitride semiconductor of a second conductivity type located on a side of the first layer (2) opposite to the gate electrode (6), a third layer (1) located between the first layer (2) and the second layer (9) and electrodes (4-5) in contact with the first layer (2) and the second layer (9).

However, because Saito's third layer (1) is non-doped GaN, Saito fails to suggest the independent Claim 12 limitation that "the third layer comprises a group III nitride semiconductor of the first conductivity type". The Claim 12 feature that the third layer comprises a group III nitride semiconductor of the first conductivity type increases the mobility of electrons. As a result, the field-effect transistor of Claim 12 has decreased ON resistance.

Because Saito fails to suggest all the limitations of independent Claims 1, 4, 5, 10, 12 and 13, the rejection over Saito should be withdrawn.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance. Applicants respectfully request favorable consideration and prompt allowance of the application.

Should the Examiner believe that anything further is necessary in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

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